

REMARKS

Claims 1-5 and 8 remain pending in the present application. The Applicants respectfully request reexamination of the present application in view of the following comments.

Allowance withdrawn

Applicants note that the indicated allowability of Claim 5 has been withdrawn. Applicants respectfully note that MPEP § 706.04 indicates, “it is unusual to reject a previously allowed claim” and instructs the Examiner that “great care” is to “be exercised in authorizing such a rejection.” Applicants regret that Claim 5 stands rejected after being found allowable, particularly as the newly cited art is unrelated to the limitations set forth in this Claim.

35 U.S.C. § 103

Claims 1-4 and 8 stand rejected under 35 USC § 103(a) as being allegedly unpatentable over Wong. (US 6,570,810, “Wong”) in view of Mokhlesi et al (US 2005/0127428, “Mokhlesi”). Applicants have reviewed the cited references and respectfully assert that embodiments in accordance with the present invention

as recited in Claims 1-4 and 8 are patentable over Wong in view of Mokhlesi for the following reasons.

The rejection alleges that “Wong discloses a tiled display structure....” Applicants respectfully traverse. Wong is directed to a contactless flash memory, and has nothing to do with display structures. Moreover, embodiments in accordance with the present claimed invention do not recite a “tiled display structure.” Applicants believe this statement to be a vestige of a prior rejection, and find such statement to have no bearing on the present subject matter.

The rejection alleges that Wong discloses “arranging multiple instances of said tile to an array covering a portion of said integrated circuit design.” The rejection further concedes that “Wong ...(is) silent about creating a tile array.” Herein, the rejection directly contradicts itself. Applicants respectfully assert that Wong is silent about tiles and arrays of tiles, in agreement with the rejection’s later position.

The rejection specifically cites to Wong Figure 3 as teaching several elements of a tile. Applicants reiterate that Wong is silent about tiles and arrays of tiles, as confirmed by the rejection itself. Moreover, Wong does not contain a Figure 3. Further, Wong Figures 3A and 3B are plan views of a

memory array, and fail to teach anything relating to layers of an integrated circuit that may be hidden beneath surface layers, e.g., a deep n-well, let alone layer structures of tiles, as recited.

With respect to Claim 1, Applicants respectfully assert that Wong in view of Mokhlesi fails to teach or suggest the claimed limitations of “merging said tiles to produce a deep N-well pattern” as recited by Claim 1, for the following reasons. While Wong may comprise a deep n-well, such deep n-well does not form a “pattern,” according to the clear meaning of the term.

For example, as shown in Wong Figures 2B and 2C, the deep n-well 204 is continuous and uniform beneath the memory array. Applicants respectfully assert that such a continuous and uniform structure is not arranged in a “pattern,” as recited. For example, a uniform white wall is generally not described as being painted in a pattern, nor is bolt of single-color material described as having a pattern. Thus, in accordance with the plain meaning of the term, Wong does not teach a “pattern” for the deep n-well.

Mokhlesi is not alleged to correct this deficiency of Wong, nor does it. For this reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 1, Applicants respectfully assert that Wong in view of Mokhlesi fails to teach or suggest the claimed limitations of “arranging multiple instances of said tile to create a tile array covering a portion of said integrated circuit design” as recited by Claim 1, for the following reasons. The rejection concedes that Wong is silent as to this element. Mokhlesi is introduced to correct this deficiency of Wong.

However, while Mokhlesi may teach some function of tiles, Mokhlesi teachings tiling with respect to circuit schematics, in contrast to an “integrated circuit design” as recited by Claim 1. For example, in [0109], Mokhlesi teaches tiling neighbor cells together horizontally and/or vertically, with reference to Figure 6. Figure 6 is a schematic of a memory array. Thus, Mokhlesi fails to teach or suggest tiling to form an “integrated circuit design” as recited by Claim 1.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 2-5 and 8 overcome the rejections of record by virtue of their dependence, and respectfully solicit allowance of these Claims.

Applicants find that the rejections of Claims 2, 3, 4 and 8 are so non-specific that Applicants are unable to constructively respond to the rejection. As previously noted, Wong Figure 3, cited by the rejection, does not exist. Figures 3A and 3B are plan view drawings, rather than cross sections, and fail to illustrate anything related to Claims 2, 3, 4 and/or 8. Applicants do not find Wong to teach first and second layers of a semiconductor structure as limited by the claimed limitations of Claims 2, 3 and 4.

Further with respect to Claim 8, Applicants respectfully assert that Wong in view of Mokhlesi fails to teach or suggest the claimed limitations of “flattening said first layer and said second layer” as recited by Claim 8, for the following reasons. Both Wong and Mokhlesi are completely silent as to the recited “flattening.” The rejection fails to cite to any teaching of the cited art alleged to present an equivalent function.

For this further reason, Applicants respectfully assert that Claim 8 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claim 5 stands rejected under 35 USC § 103(a) as being allegedly unpatentable over Wong. (US 6,570,810, “Wong”) in view of Mokhlesi et al (US

2005/0127428, “Mokhlesi”) and further in view of Lee et al., (US 5,913,122, “Lee”). Applicants have reviewed the cited references and respectfully assert that embodiments in accordance with the present invention as recited in Claims 1-4 and 8 are patentable over Wong in view of Mokhlesi and further in view of Lee for the following reasons.

Applicants respectfully assert that Claim 5 overcomes the rejections of record by virtue of its dependence, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 5, Applicants respectfully assert that Wong in view of Mokhlesi and further in view of Lee fails to teach or suggest the claimed limitations of “editing said tile array” as recited by Claim 5, for the following reasons. The rejection concedes that Wong in view of Mokhlesi fail to “mention editing the tile array.” Lee is introduced to correct this deficiency of Wong in view of Mokhlesi.

The sole teaching of any editing operation in Lee is “[t]hus the only edit is the N-well to P-substrate Junction.” As the remainder of the paragraph deals with concentration of dopants, Applicants respectfully assert that the cited passage of Lee refers to editing a production process to change a doping level, in

contrast to having any relation to the claimed limitations of “editing said tile array” as recited by Claim 5.

For this additional reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Furthermore, Lee is directed to a single FET structure, in contrast to an array. Thus, one of ordinary skill in the art would find Lee’s teachings to be directed to a single FET structure, and not to an “array,” as recited.

For this further reason, Applicants respectfully assert that Claim 5 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

CONCLUSION

Claims 1-5 and 8 remain pending in the present application. The Applicants respectfully request reexamination of the present application in view of the remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

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